REMARKS

Applicant has reviewed and considered the Office Action mailed on December 22, 2004, and the references cited therewith.

Claims 1, 3, and 22 are amended and claim 31 is added; as a result, claims 1-5, 9-15, 22, 26-29, and 31 are now pending in this application.

§102 Rejection of the Claims

Claims 1-5, 9-10, 13-15, 22 and 26 were rejected under 35 USC § 102(e) as being anticipated by Park et al. (U.S. Patent No. 6,566,927).

Claim 1 has been amended herein to further define the first transistor of the first stack of transistors as being "directly connected to said first storage node." Thus, in claim 1, the transistor that is receiving the clock signal is the one that is directly connected to the first storage node and the transistor that is receiving the delayed, inverted version of the clock signal that is output by the NOR gate is the one that is not directly connected to the first storage node. In Fig. 12 of Park et al., the clock (Clk) is delivered to the transistors that are not directly connected to the corresponding storage nodes and the delayed, inverted clock (Clkb) that is output by the NOR gate 1213 is delivered to the transistors that are directly connected to the corresponding storage nodes.

Based on the foregoing, it is submitted that claim 1, as amended, is not anticipated by Park et al. Reconsideration and allowance of claim 1 is therefore respectfully requested.

Claims 2-5, 9-10, and 13-15 are dependent claims that depend either directly or indirectly from independent claim 1. Consequently, these claims are allowable for at least the same reasons as independent claim 1. One or more of these claims also provide further bases for patentability. For example, claim 3 has been amended to further define the third transistor of the second stack of transistors as being "directly connected to said first storage node." As stated above, in Fig. 12 of Park et al., the clock (Clk) is delivered to the transistors that are not directly connected to the corresponding storage nodes and the delayed, inverted clock (Clkb) that is output by the NOR gate 1213 is delivered to the transistors that are directly connected to the corresponding storage nodes.

Claim 22 has been amended herein to further define the first transistor of the first transistor stack as being "directly connected to said first storage node" and the third transistor of the second transistor stack as being "directly connected to said second storage node." As described above, these features are not disclosed within Park et al.

Based on the foregoing, it is submitted that claim 22, as amended, is not anticipated by Park et al. Reconsideration and allowance of claim 22 is therefore respectfully requested.

Claim 26 is a dependent claim that depends directly from independent claim 22. Consequently, this claim is allowable for at least the same reasons as independent claim 22.

New Claims

New claim 31 has been added. Claim 31 is a dependent claim that depends directly from independent claim 27. Consequently, claim 31 is allowable for at least the same reasons as independent claim 27. Claim 31 also provides further basis for patentability. That is, claim 31 further defines the first pull up transistor of claim 27 as being larger than the second pull up transistor. None of the references cited by the Examiner disclose separate pull up paths using different size transistors.

Allowable Subject Matter

Claims 11-12 and 27-29 were allowed.

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111 Serial Number: 10/616,810 Filing Date: July 10, 2003 Title: SLAVE-LESS EDGE-TRIGGERED FLIP-FLOP

Assignee: Intel Corporation

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Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (480-948-3745) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-2359.

Respectfully submitted,

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Date 2/22/05

John C. Scott

// Reg. No. 38,613

<u>CERTIFICATE UNDER 37 CFR 1.8:</u> The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this ...day of <u>February</u>, 2005.

MEREDITH MESCHER

Name

Signature